

### 4.7.1 Access Control as a Function of Address and Operating Mode

Table 4-4 describes the action taken by the processor for each section of the 64-bit address space as a function of the operating mode of the processor, including the selection of a TLB Refill vector and other special-case behavior.

**Table 4-4 Address Space Access and TLB Refill Selection as a Function of Operating Mode**

Virtual Address Range	Segment Name(s)	Action when Referenced from Operating Modes		
		User Mode	Supervisor Mode	Kernel Mode
<p><i>SEGBITS</i> = 40, <i>PABITS</i> = 36</p>				
0xFFFF FFFF FFFF FFFF through 0xFFFF FFFF E000 0000	kseg3	Address Error	Address Error	Mapped  Refill Vector: TLB (KX=0) XTLB(KX=1)  See <a href="#">Section 4.7.5, "Address Translation in Debug Mode"</a> on page 75 for special behavior when Debug <sub>DM</sub> = 1
0xFFFF FFFF DFFF FFFF through 0xFFFF FFFF C000 0000	sseg, ksseg	Address Error	Mapped  Refill Vector: TLB (KX=0) XTLB(KX=1)	Mapped  Refill Vector: TLB (KX=0) XTLB(KX=1)
0xFFFF FFFF BFFF FFFF through 0xFFFF FFFF A000 0000	kseg1	Address Error	Address Error	Unmapped, Uncached  See <a href="#">Section 4.7.2, "Address Translation and Cache Coherency Attributes for kseg0 and kseg1"</a> on page 72
0xFFFF FFFF 9FFF FFFF through 0xFFFF FFFF 8000 0000	kseg0	Address Error	Address Error	Unmapped  See <a href="#">Section 4.7.2, "Address Translation and Cache Coherency Attributes for kseg0 and kseg1"</a> on page 72
0xFFFF FFFF 7FFF FFFF through 0xC000 00FF 8000 0000		Address Error	Address Error	Address Error
0xC000 00FF 7FFF FFFF through 0xC000 0000 0000 0000	xkseg	Address Error	Address Error	Address Error if KX = 0  Mapped if KX = 1  Refill Vector: XTLB